Total No. of questions: 11

F-4/2110

9820/NJ

COMPUTER ARCHITECTURE
SUBJECT CODE: CPE-201

TIME:03 HOURS

MAX.MARKS:50

INSTRUCTIONS TO CANDIDATES:

- Attempt any three questions from SECTION-A and any three from section B. Each question carries 5 marks.
- SECTION-C is compulsory. Each question carries 2 marks.

Section A

Q1 Discuss instruction cycle of a basic computer with a neat diagram. (5)
Q2 Design a four-bit combinational shifter to perform shift micro-operations. (5)
Q3 What are addressing modes? Explain the various addressing modes with examples. (5)
Q4 Explain address sequencer of the microprogrammed control unit with a detailed diagram. (5)
Q5 Explain Booth's algorithm with a detailed flowchart. (5)

Section B

Q6. Write a short note on Set-Associative mapping. (5)
Q7. How RAM and ROM chips are connected to CPU through data and address buses. (5)
Q8. Discuss DMA controller. (5)
Q9. What are the benefits of parallel processing? Explain Flynn's classification for parallel computers. (5)
Q10. Discuss the concept of cache coherence in detail. (5)

Section C

Q11

i. What is the use of EEPROM?
ii. What are shift micro-operations?
iii. What is the control bus?
iv. Which registers are involved in a fetch phase of instruction cycle?
v. What are MIMD computers?
vi. Differentiate between memory-mapped I/O and isolated I/O.
vii. What is the difference between selective set and selective complement logical micro-operations?
viii. What is a control memory?
ix. What is the need of I/O interface unit?
x. Write a short note on DMA Modes.

10 X 2 = 20